

REMARKS

I. Introduction

Claims 2 and 13 have previously been cancelled without prejudice.

Claims 1, 7, 9, and 17 have been amended, and claim 27 has been added, to more particularly define the claimed invention.

No new matter has been added by the amendments to the claims.

Claims 3-6, 8, 10-12, 14-16, and 18-26 are also pending in the case.

Claims 1, 3-6, and 17-19 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Tsai et al. U.S. Patent 6,157,266 (hereinafter "Tsai").

Claims 20-22 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of Horan et al. U.S. Patent 6,462,623 (hereinafter "Horan").

Claims 23-26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai.

Claims 7-10 have been objected to as being dependent upon a rejected base claim.

Claims 11, 12, and 14-16 have been allowed.

Reconsideration of this application in light of the following Remarks is hereby respectfully requested.

II.. The Objections to the Claims

The Examiner objected to claims 7-10 as being dependent upon a rejected base claim. Claims 7 and 9 have been rewritten in independent form because the Examiner has indicated in the Office Action that these claims contain allowable subject matter. Therefore, amended claim 7, claim 8 that depends from claim 7, amended claim 9, and claim 10 that depends from claim 9 should now be allowable.

No new matter has been added by these claim amendments.

III. The Rejections Based on 35 U.S.C. § 102

Claims 1, 3-6, and 17-19 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Tsai. These rejections are respectfully traversed.

Claims 1 and 3-6

The variable delay cell of applicants' amended independent claim 1 defines a delay cell that includes a switching transistor (e.g., transistor SW1 of FIG. 4) connected in series between a plurality of load resistance transistors (e.g., transistors RL1a, RL1b, ..., RL1n of FIG. 4) and a plurality of bias current transistors (e.g., transistors ICONTa, ICONTb, ..., ICONTn of FIG. 4), switching circuitry (e.g., multiplexer 110b of FIG. 4) "configured to selectively operatively connect at least a first one of the load resistance transistors in parallel with at least one other of the load resistance transistors," and "other switching circuitry" (e.g., multiplexer 110n of FIG. 4) "configurable to selectively operatively connect at least a second one of the load resistance transistors in parallel with the at least one other of the load resistance transistors." Therefore, claim 1 provides for multiple separate switching circuitries for selectively operatively connecting multiple load resistance transistors in parallel with one another. These switching circuitries of the present invention allow "the number of the load resistance transistors that are actually operating in parallel to be selected," which "allows the operating range (i.e., the time delay characteristic) of the delay cell to be greatly extended" (applicants' specification, page 2, lines 12-20). Also see applicants' specification, page 9, lines 30-33, for example.

Nowhere does Tsai show or suggest "switching circuitry configured to selectively operatively connect at least a first one of the load resistance transistors in parallel with at least one other of the load resistance transistors" and "other switching circuitry configurable to selectively operatively connect at least a second one of the load resistance transistors in parallel with the at least one other of the load resistance transistors," as required by applicants' amended claim 1. Instead, FIGS. 1 and 2 of Tsai show a "first signal controlled active load [that] comprises a pair of drain coupled transistors, wherein one member of the pair has a gate coupled with the second control signal, VCO_P, and the other member has a gate coupled with the second bias signal, BIAS_P." Tsai, column 3, lines 40-43. This second bias signal, BIAS_P, is "held substantially constant," and only second control signal, VCO_P, is controllable to connect the pair of transistors of the first signal controlled active load. Tsai, column 2, line 65.

Therefore, Tsai's signal control active load does not include a plurality of transistors, switching circuitry configured to selectively operatively connect at least a first one of its transistors in parallel with at least one other of its transistors, and "other switching circuitry configurable to selectively operatively connect at least a second one of the load resistance transistors in parallel with the at least one other of the load resistance transistors," as required by applicants' independent claim 1, but instead includes only a pair of transistors controlled by one control signal, VCO_P. Nothing like the "switching circuitry" and the "other switching circuitry," thus defined by applicants' claim 1, is shown or suggested in Tsai.

Claim 1, as amended, is therefore not anticipated by Tsai. Applicants respectfully submit that independent claim 1, claims 3-6, additional claim 27, and any other claims dependant from claim 1 are allowable over Tsai.

Claims 17-19

The differential delay cell of applicants' amended independent claim 17 defines a delay cell comprising a plurality of first load resistance transistors connected in parallel with one another, a plurality of second load resistance transistors connected in parallel with one another, and a plurality of bias current transistors connected in parallel with one another, wherein at least one of the following is true: "1) the plurality of first load resistance transistors and the plurality of second load resistance transistors each includes at least three load resistance transistors; and 2) the plurality of bias current transistors includes at least three bias current transistors."

As described above, Tsai's first signal controlled active load includes only a pair of drain coupled transistors, which is also true of Tsai's second signal controlled active load. Furthermore, Tsai's first and second signal controlled current sources each only includes a single transistor, transistors 115 and 125, respectively. See, Tsai, FIG. 2 and column 3, lines 16-38. Nowhere does Tsai show or suggest that either the number of transistors included in each of the first and second controlled active loads or the combined number of transistors included in the signal controlled current sources is at least three.

Claim 17, as amended, is therefore not anticipated by Tsai. Applicants respectfully submit that independent claim 17, claims 18-26, and any other claims dependant from claim 17 are allowable over Tsai.



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IV. The Rejection Based on 35 U.S.C. § 103

Claims 20-22 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of Horan, and claims 23-26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai. The Examiner's rejection is respectfully traversed.

Claims 20-22

As applicants have pointed out above, independent claim 17 is patentable over Tsai. For at least the foregoing reasons, claims 20-22, which depend from claim 17, are patentable over Tsai in view of Horan.

Claims 23-26

As applicants have pointed out above, independent claim 17 is patentable over Tsai. For at least the foregoing reasons, claims 23-26, which depend from claim 17, are patentable over Tsai.

V. Conclusion

The foregoing demonstrates that claims 1, 3-12, and 14-27 are allowable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,

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